

FIG. 1 (a)

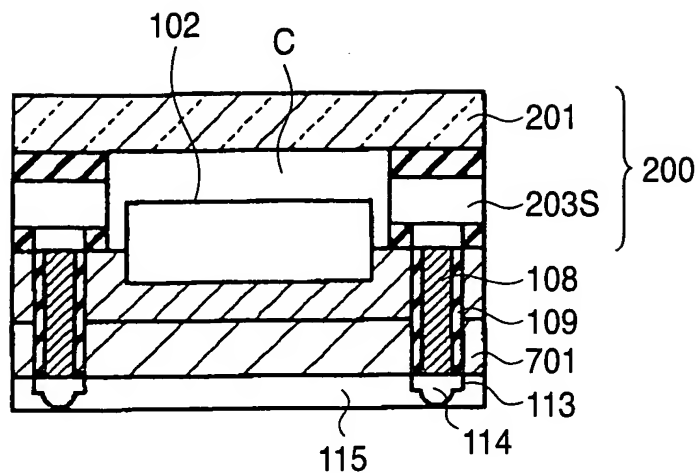


FIG. 1 (b)

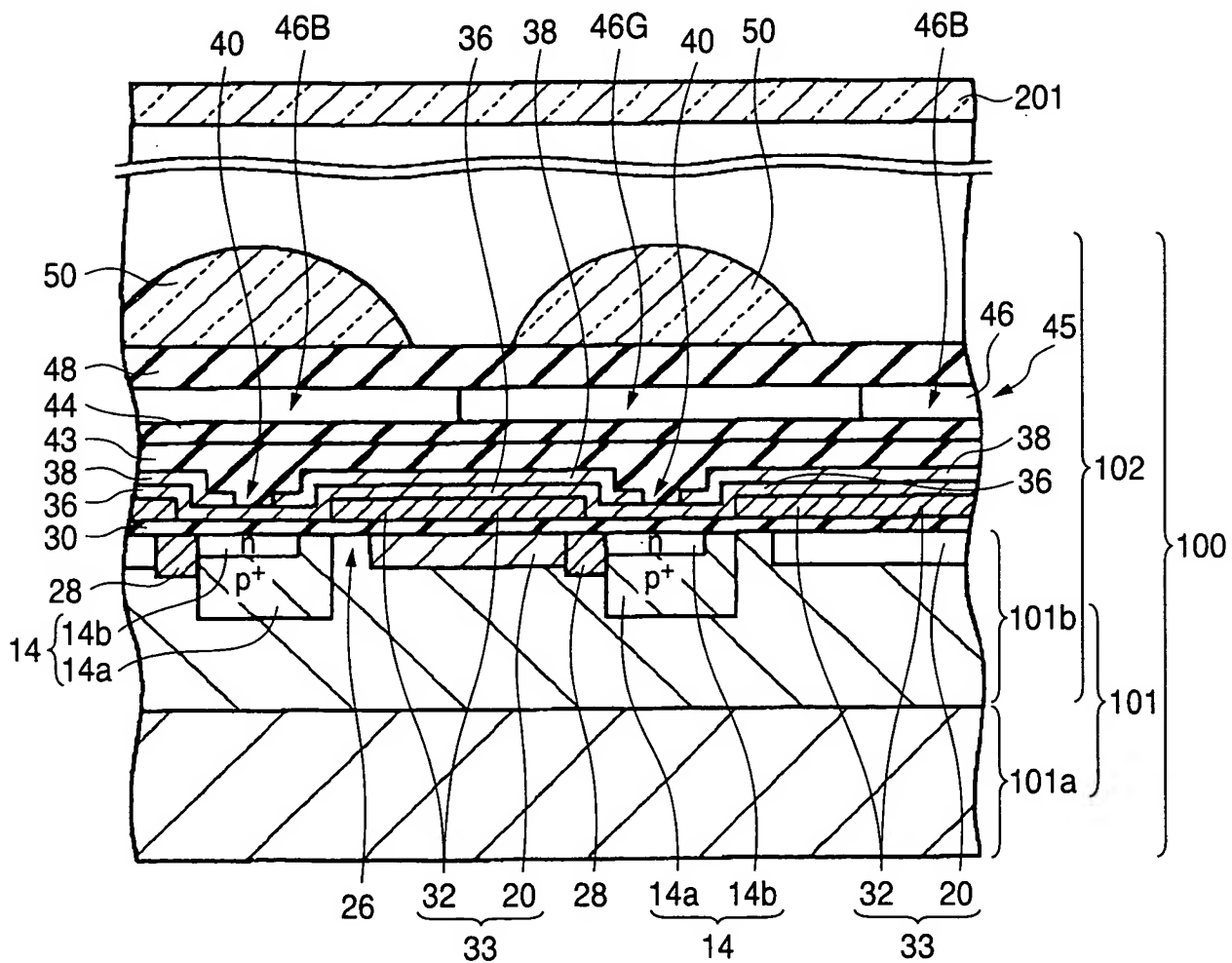


FIG. 2 (a)

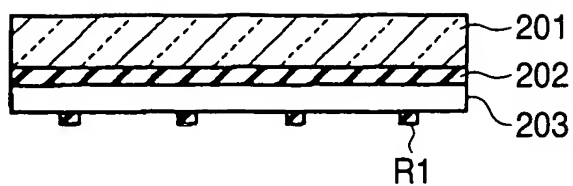


FIG. 2 (b)

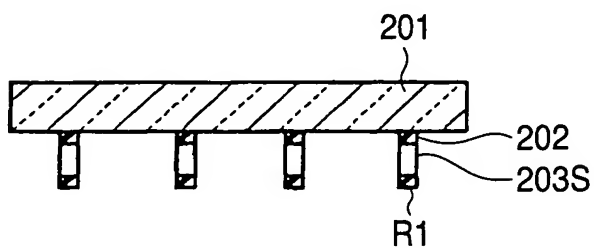


FIG. 2 (c)

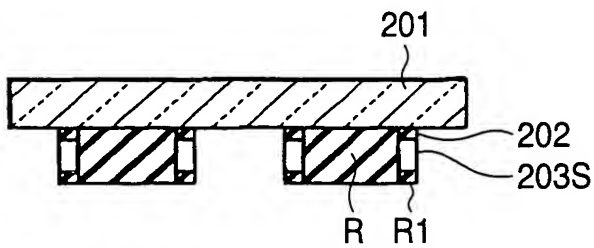


FIG. 2 (d)

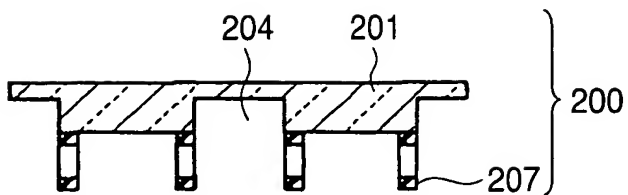




FIG. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 701, a first insulating layer 101, and a second insulating layer 201. A central region contains a conductive layer 207. This central region is surrounded by a first insulating layer 202, which is further surrounded by a second insulating layer 203S. The second insulating layer 203S is formed on the first insulating layer 202 and the conductive layer 207. The second insulating layer 203S is formed on the first insulating layer 202 and the conductive layer 207. The second insulating layer 203S is formed on the first insulating layer 202 and the conductive layer 207.

Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a central region C, a central layer 201, a central layer 202, a central layer 203S, a central layer 207, a base layer BP, a base layer 108, a base layer 109, and a base layer 701. The device is labeled H.

FIG. 4 (a)

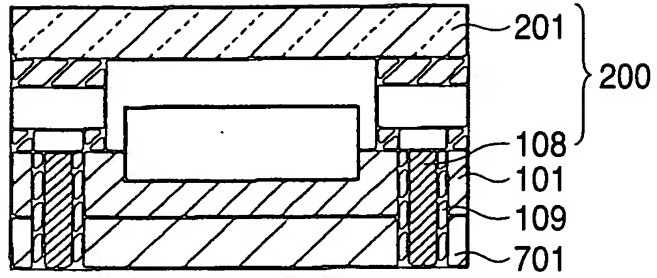


FIG. 4 (b)

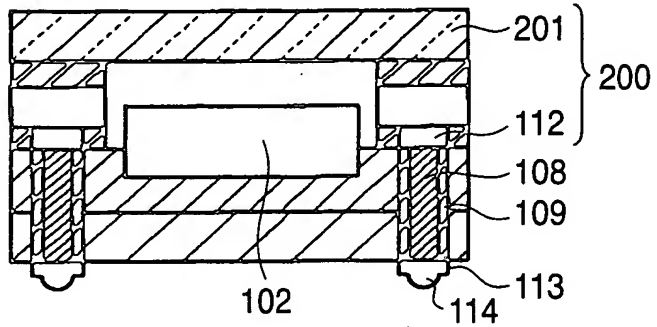


FIG. 4 (c)

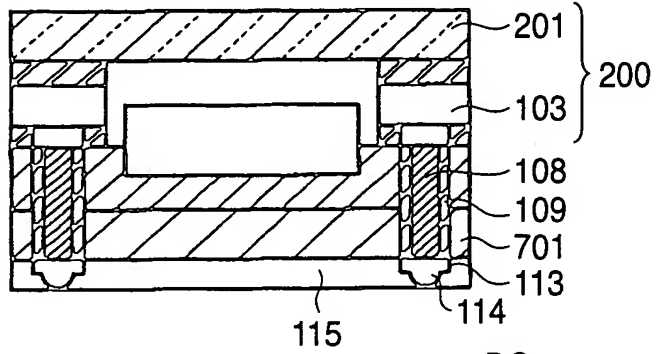


FIG. 4 (d)

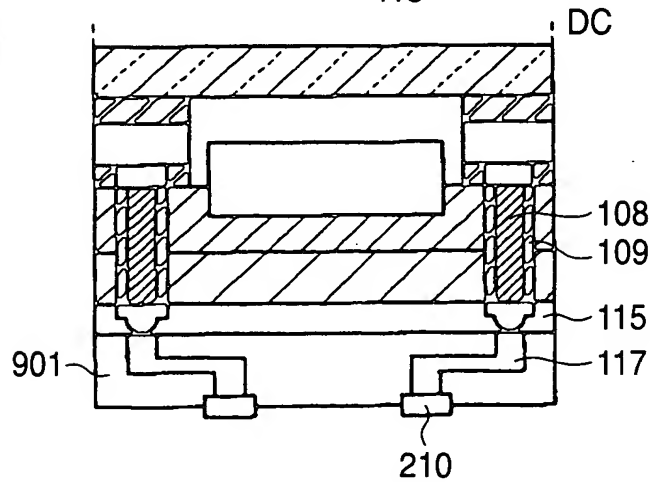


FIG. 5 (a)

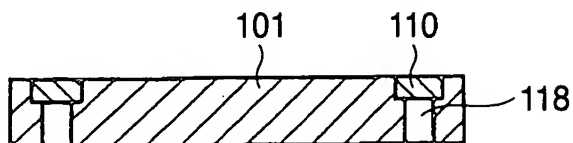


FIG. 5 (b)

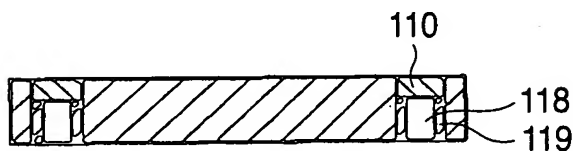


FIG. 5 (c)

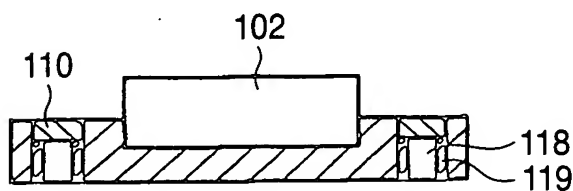


FIG. 5 (d)

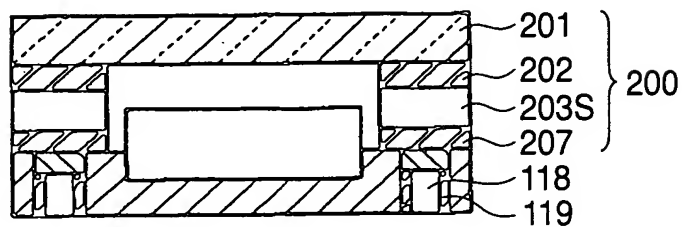


FIG. 5 (e)

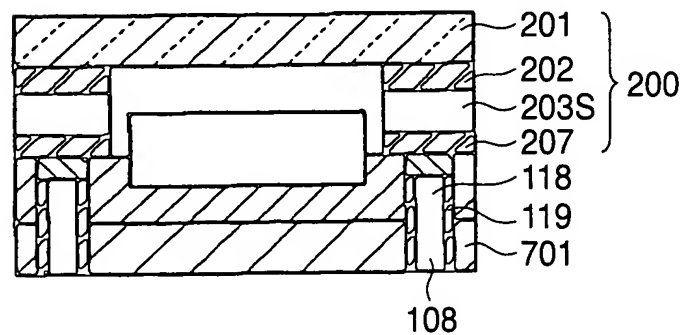


FIG. 6 (a)

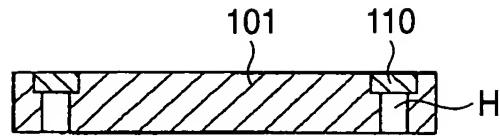


FIG. 6 (b)

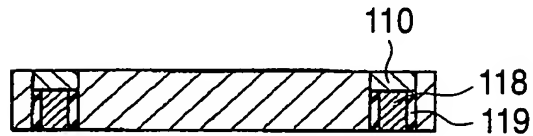


FIG. 6 (c)

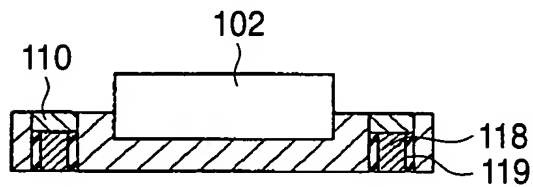


FIG. 6 (d)

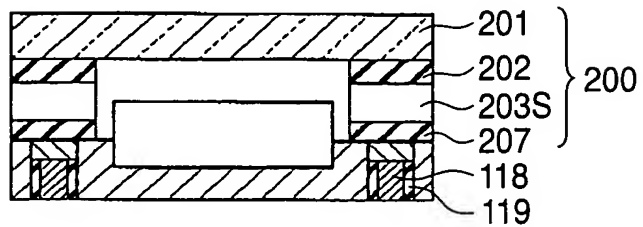


FIG. 6 (e)

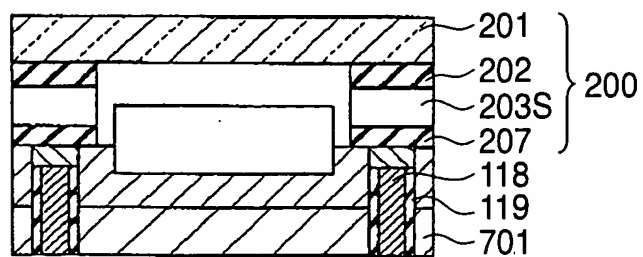


FIG. 7 (a)

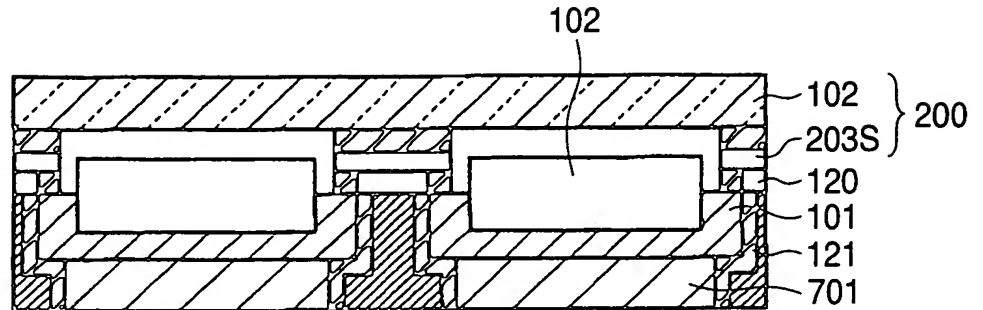


FIG. 7 (b)

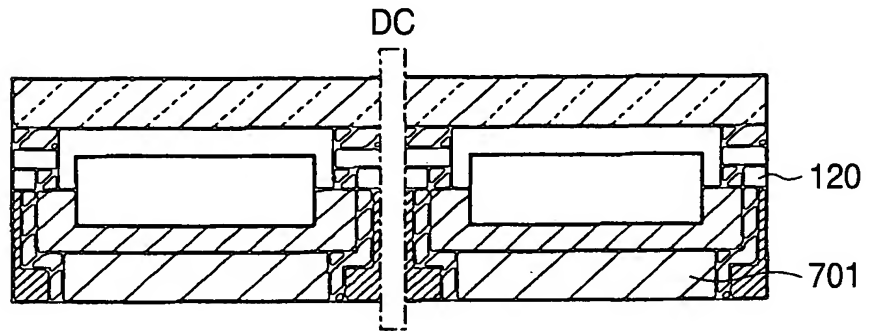


FIG. 8

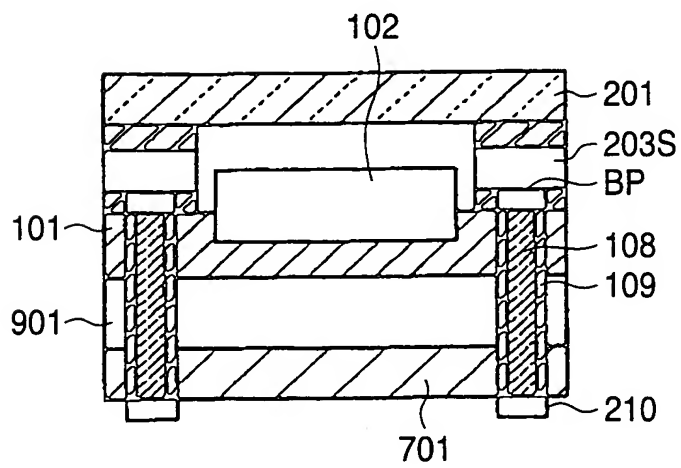


FIG. 9

